## AMENDMENTS TO THE CLAIMS

LISTING OF CLAIMS

1. (previously presented) A semiconductor package comprising:

a substrate comprising a first side, an opposing second side, a plurality of die contacts on the first side comprising first multi layer metal bumps having first planar tip portions;

a semiconductor die on the first side comprising a plurality of pads bonded to the first planar tip portions of the die contacts;

a plurality of conductors on the second side in electrical communication with the die contacts having a plurality of bonding sites thereon in an area array; and

a plurality of external contacts on the second side comprising second multi layered metal bumps having second planar tip portions, each external contact comprising a first metal layer on a bonding site, a metal bump on the first metal layer having a planar tip portion, and a non-oxidizing outer layer on the metal bump.

2. (previously presented) The semiconductor package of claim 1 wherein the die contacts and the external contacts comprise generally pyramidally shaped metal bumps.

3. (withdrawn) The semiconductor package of claim 1 wherein the die is back bonded to the first side and wire bonded to the die contacts.

4. (previously presented) The semiconductor package of claim 1 wherein the conductors and the bonding sites comprise copper, the first metal layer comprises copper,

the metal bump comprises nickel, and the non-oxidizing outer layer comprises gold.

5. (previously presented) The semiconductor package of claim 1 wherein the substrate comprises a material selected from the group consisting of organic polymer materials, epoxy resins, and polyimide resins.

6. (withdrawn) The semiconductor package of claim 1 wherein the die is wire bonded to the die contacts in a chip-on-board configuration.

7. (withdrawn) The semiconductor package of claim 1 wherein the die is wire bonded to the die contacts in a board-on-chip configuration.

8. (withdrawn) The semiconductor package of claim 1 wherein the substrate includes a recess and the die is contained in the recess in contact with a metal heat spreader.

9. (currently amended) A semiconductor package comprising:

a substrate having a first side and an opposing second side;

a plurality of die contacts on the first side in a pattern, and a plurality of external contacts on the second side in an area array in electrical communication with the die contacts, each die contact and each external contact comprising a multi layered metal bump having a planar tip portion;

each die contact and each external contact comprising a base metal layer, a pyramidally shaped metal bump on the base metal layer and a non-oxidizing outer metal layer on the metal bump; and

a semiconductor die flip chip mounted to the first side having a plurality of pads in the pattern bonded to the die contacts.

[;]

~~each external contact having a height less than that of a solder ball external contact having a diameter of from 0.3 mm to 0.762 mm.~~

10. (previously presented) The semiconductor package of claim 9 further comprising an encapsulant on the substrate encapsulating the die and the first side.

11. (previously presented) The semiconductor package of claim 9 wherein the base metal layer comprises copper, the metal bump comprises nickel, and the non-oxidizing outer metal layer comprises gold.

12. (previously presented) The semiconductor package of claim 9 wherein a height H of each die contact and each external contact is about 5 $\mu$m.

13. (previously presented) The semiconductor package of claim 9 further comprising a solder mask on the second side configured to electrically insulate the external contacts.

14. (currently amended) A semiconductor package comprising:

a substrate having a first side, and an opposing second side;

a plurality of die contacts on the first side comprising first multi layered metal bumps in a pattern having generally planar first tip portions;

a plurality of conductors on the second side having a plurality of bonding sites in an area array in electrical communication with the die contacts;

a plurality of external contacts on the bonding sites in electrical communication with the die contacts comprising second multi layered metal bumps having generally planar second tip portions; and

~~, with a spacing S of the external contacts larger than the spacing of solder ball external contacts having a diameter of from 0.3 mm to 0.762 mm; and~~

a semiconductor die flip chip mounted to the substrate, the die comprising a plurality of pads in the pattern bonded to the die contacts.

15. (previously presented) The semiconductor package of claim 14 wherein each first multi layered metal bump and each second multi layered metal bump comprises a copper layer, a nickel bump and a gold layer.

16. (previously presented) The semiconductor package of claim 14 further comprising an encapsulant on the substrate encapsulating the die.

17. (previously presented) The semiconductor package of claim 14 wherein the bonding sites and the external contacts are in a grid array.

Claims 18-57 (canceled).

58. (previously presented) An electronic assembly comprising:

a supporting substrate comprising a plurality of electrodes;

at least one semiconductor package on the supporting substrate comprising:

a substrate comprising a plurality of die contacts on a first side thereof having first planar tip portions and a plurality of conductors on a second side

thereof in electrical communication with the die contacts having a plurality of bonding sites in an area array;

a semiconductor die on the substrate comprising a plurality of pads bonded to the die contacts on the substrate; and

a plurality of external contacts on the bonding sites bonded to the electrodes on the substrate comprising multi layered metal bumps having second planar tip portions configured to facilitate bonding to the electrodes on the supporting substrate, to reduce a thickness of the package on the supporting substrate, and to insure a planarity of the package on the supporting substrate relative to solder ball external contacts, each external contact including a first metal layer on a bonding site, a metal bump on the first metal layer, and a non-oxidizing outer layer on the metal bump.

59. (previously presented) The assembly of claim 58 wherein the substrate and the package are configured as a multi chip module.

60. (previously presented) The assembly of claim 58 wherein the first metal layer comprises copper, the metal bump comprises nickel, and the non-oxidizing outer layer comprises gold.

61. (previously presented) The assembly of claim 58 wherein the die contacts comprise second multi layer metal bumps.

62. (currently amended) An electronic assembly comprising:

a supporting substrate comprising a plurality of electrodes; and

a semiconductor package comprising a substrate having a first side and an opposing second side, a plurality of

die contacts on the first side comprising first multi layered metal bumps having generally planar first tip portions, a plurality of conductors having bonding sites on the second side in an area array in electrical communication with the die contacts, a semiconductor die bonded to the die contacts in a flip chip configuration, and a plurality of external contacts on the bonding sites comprising second multi layer metal bumps having generally planar second tip portions bonded to the electrodes, each external contact having a height H on the substrate.

~~less than that of solder ball external contacts having a diameter of from 0.3 mm to 0.762 mm, and a spacing S substantially larger than that of the solder ball external contacts.~~

63. (currently amended) The assembly of claim 62 wherein each die contact comprise a copper layer, a nickel bump and a gold layer, and each external contact comprises a copper layer, a nickel bump and a gold layer.

64. (currently amended) The assembly of claim 62 wherein the height H is about 5 μm.

~~each external contact comprise a copper layer, a nickel bump and a gold layer.~~